LDPC Decoder with a Limited-Precision FPGA-based Floating-Point Multiplication Coprocessor

Computational Science Research Center

Raymond Moberly, doctoral candidate

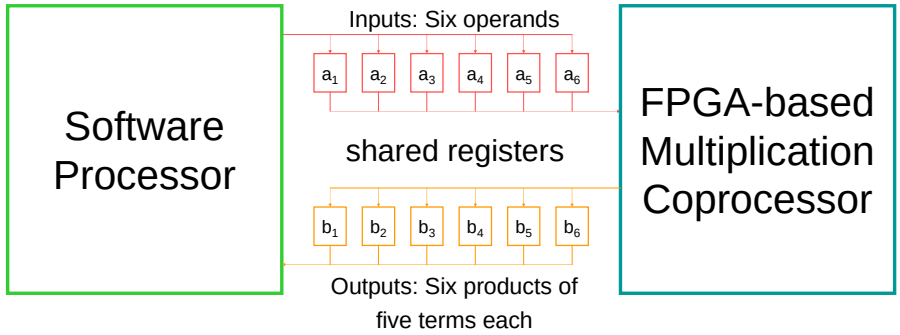
with Professors Michael O'Sullivan and Khurram Waheed

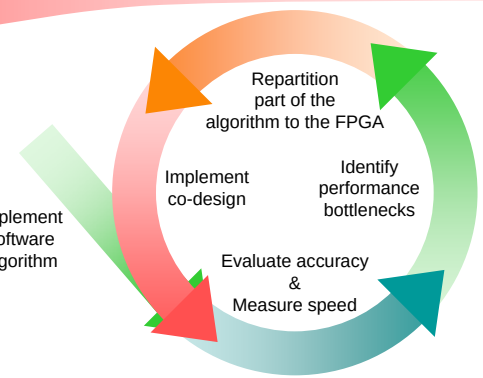
San Diego State University

FPGA as a Computational Coprocessor

The Sum-Product algorithm, used for LDPC decoding of a (6,3)-regular code, performs repeated computations of product terms. A frequently repeated function computes six output products (of five terms each) from six inputs.

The partitioned function is allocated to the programmable logic portion of the co-design.



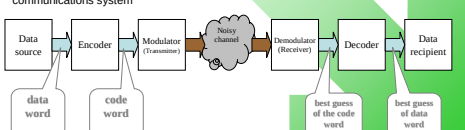


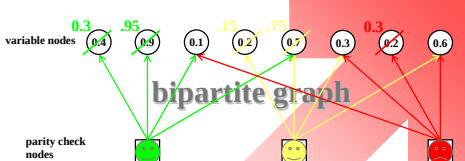
The Altera SOPC development environment allows for iterative development of a computational algorithm, implemented in a software / programmable logic co-design

Interdisciplinary Research

Communications

The Decoder presents the greatest computational challenges in a communications system





Numerical Analysis

$$| \hat{a} - a | \le \varepsilon_a$$

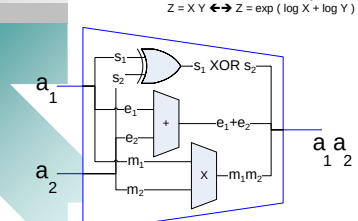
$$| \Pi_i \hat{a}_i - \Pi_i a_i | \le \varepsilon_\Pi$$

The established bounds upon the precision of operands directly determines the precision of computational results.

Our computational research considers nonlinear scales for limited precision numbers. The logic circuitry required for the implementing the mathematical operations is considered.

The computation of a product is mathematically equivalent to the computation of the exponential of a sum of logarithms:

Z = X Y ↔ Z = exp (log X + log Y)



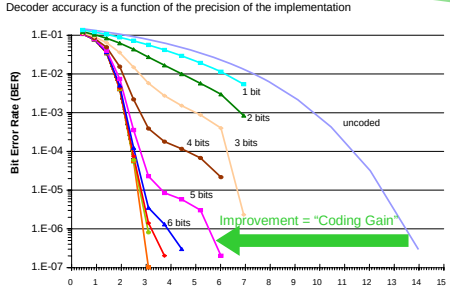
Algorithms / Graph Theory

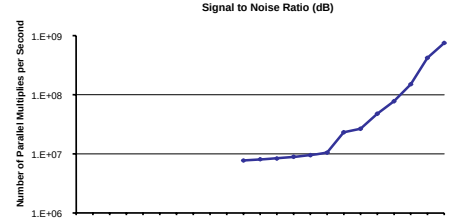
The Sum-Product Algorithm is known outside of the signal processing community as Pearl's Belief Propagation. It is iterative – until parity is achieved or a limit is reached.

Computer Architecture

The FPGA permits construction of computation with prescribed precision, allows parallel operations, and representations other than traditional integer and floating point formats.

Decoder accuracy is a function of the precision of the implementation





Decoder speed is dependent on the precision of the implementation

An acceptable bit error rate limit is a meaningful engineering criteria for a communications channel. Compare curves at a specified BER (where they intersect a horizontal equal-error-rate line) – the horizontal difference between curves is referred to as the *coding gain*. The uncoded simulation serves as the baseline against which coding gain is measured.

How much coding gain is achievable for each choice of mantissa precision in the iterative decoder is a tradeoff versus the number of multiplications that the FPGA is capable of performing. The example LDPC code has 1000 parity-check nodes, each parity-check computation requires six of the 5-operand multiplies to be performed, and the decoder runs for 10 iterations; that works out to 60,000 operations. The coding gain per second of computation for this example code has been computed and is shown in the following figure.

Achievable coding gain per unit time of FPGA-based computation

(synthesized for a Xilinx XC2VP2-7fg256 FPGA)