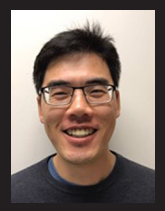
RISP: An Energy-Aware Reconfigurable In-Storage Processing Framework for Big Data Analysis



Existing in-storage processing (ISP) techniques focus on maximizing data processing rate by always utilizing all storage resources. We find that this "always running in full gear" strategy wastes energy for some applications. In this paper we propose RISP (Reconfigurable ISP), an energy-aware ISP framework that employs FPGA as data processing cells and NVM controllers. It can reconfigure storage resources based on an application's data processing complexity so that a high performance and energyefficiency can be achieved simultaneously. RISP is modeled and then validated on an FPGA board. Experimental results show that compared with traditional host CPU-based processing RISP (with 16 channels or more) improves performance by 1.6-25.4× while saving energy by a factor of 2.2-161. Further, it outperforms a state-of-the-art ISP technique iSSD by up to a factor of 14.6 while saving energy by a factor of 1.6. Its reconfigurability could provide up to 77.2% additional energy saving.

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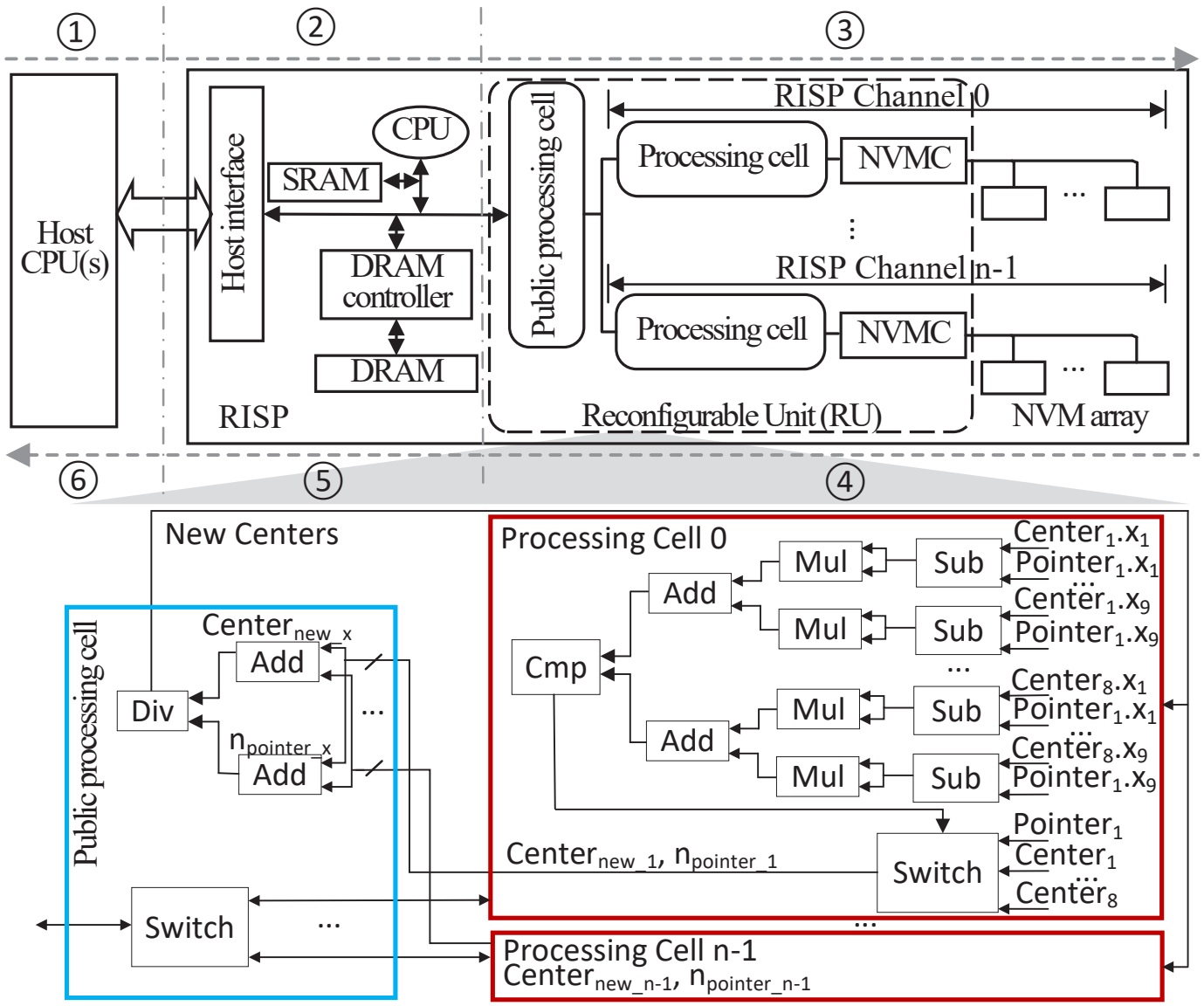
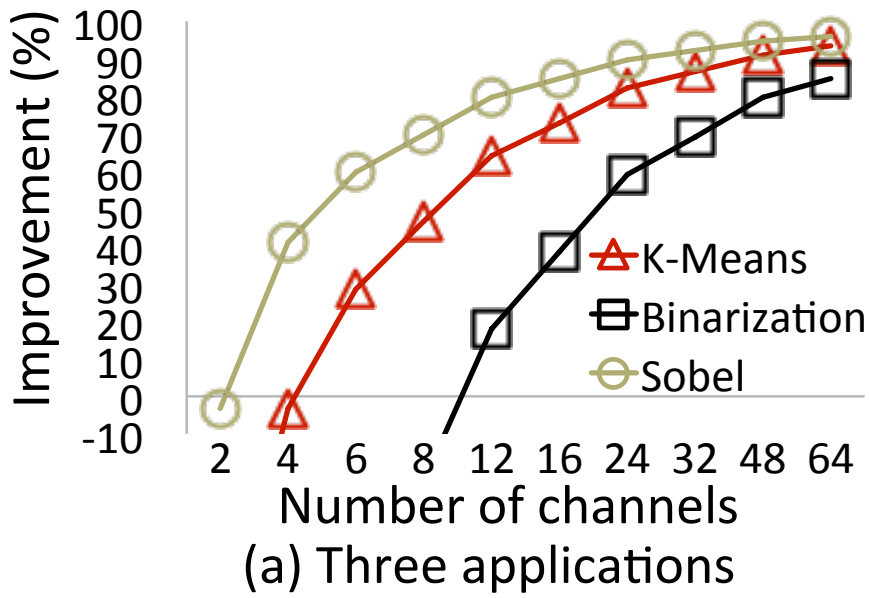
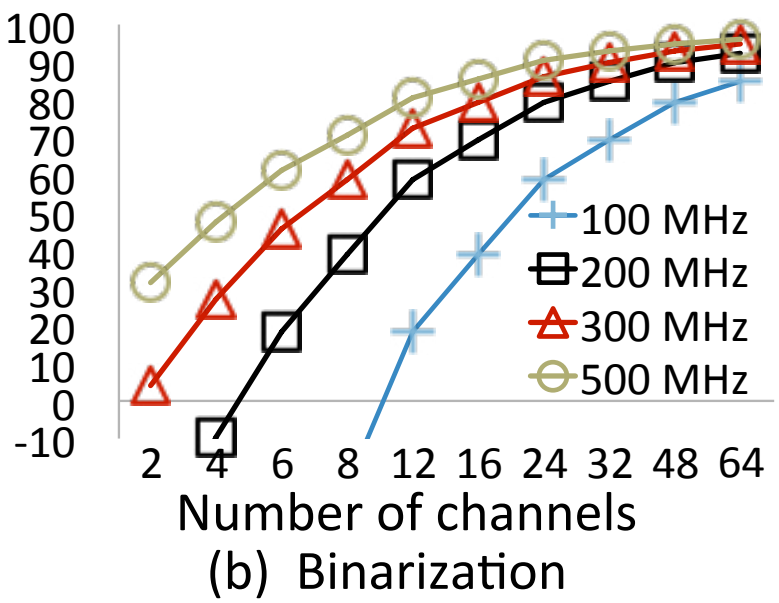




(a) Three applications



(b) Binarization